Patent Claims

1. A high speed processor having:

a data processing unit (13) for processing data;

a data memory (20) which is connected to the data processing unit via a data bus (10) and can be addressed by the data processing unit (13) via a data memory address bus (18);

at least one input interface buffer (9) which is connected to the data bus (10) and has the purpose of buffering input data;

at least one output interface buffer (26) which is connected to the data bus (10) and has the purpose of buffering output data,

the input interface buffer (9) and the output interface buffer (26) being directly addressable by the data processing unit (13) via an interface address bus (24).

2. The high speed processor as claimed in claim 1, wherein the data memory (20) contains at least one RAM memory (19).

3. The high speed processor as claimed in claim 1 or 2, wherein the data processing unit (13) is connected to a ROM memory (15) which stores program data.

4. The high speed processor as claimed in one of the preceding claims, wherein the data processing unit (13) is an RISC data processing unit.

5. The high speed processor as claimed in one of the preceding claims, wherein the data processing unit (13) contains a plurality of addressable internal registers.

6. The high speed processor as claimed in one of the preceding claims, wherein the data processing unit (13) can carry out a plurality of data transfer processor commands in order to directly exchange data between the data memory (20), the registers (14) and the interface buffers (9, 26).

7. The high speed processor as claimed in one of the preceding claims, wherein when a first data transfer processor command is carried out by the data processing unit (13), the input data buffered in the input interface buffer (9) is transmitted directly into an internal register (14) for data processing.

8. The high speed processor as claimed in one of the preceding claims, wherein when a second data transfer processor command is carried out by the data processing unit (13), the input data buffered in the input interface buffer is transmitted directly into an output interface buffer (26) for the outputting of data.

9. The high speed processor as claimed in one of the preceding claims, wherein when a third data transfer processor command is carried out by the data processing unit (13), the data buffered in an internal register (14) of the data processing unit (13) is transmitted directly into the output interface buffer (26) for the outputting of data.

10. The high speed processor as claimed in one of the preceding claims, wherein when a fourth data

transfer processor command is carried out, the input data buffered in an input interface buffer (9) is transmitted directly into the data memory (20) for storage.

11. The high speed processor as claimed in one of the preceding claims, wherein when a fifth data transfer processor command is carried out by the data processing unit (13), the data stored in the data memory (20) is transmitted directly into the output interface buffer (26) for the outputting of data.

12. The high speed processor as claimed in one of the preceding claims, wherein the input interface buffer (9) is connected to an analog/digital converter (5).

13. The high speed processor as claimed in one of the preceding claims, wherein the output interface buffer (26) is connected to a D/A converter (32).

14. The high speed processor as claimed in one of the preceding claims, wherein the input interface buffer (9) and the output interface buffer (26) are connected to the data processing unit (13) via a control signal bus.

15. The high speed processor as claimed in one of the preceding claims, wherein the input interface buffer (9) is an xDSL interface buffer for buffering xDSL data.

16. The high speed processor as claimed in claim 15, wherein the xDSL input interface buffer (9) has a data frame detecting device for detecting a data frame synchronization data pattern.

17. The high speed processor as claimed in claim 16, wherein the data frame detecting device has a shift register for writing in input data, a data pattern memory for storing the data frame synchronization data pattern and a comparator device for bit-by-bit data comparison of the input data written into the shift register, and of the data frame synchronization data pattern stored in the data pattern memory,
the comparator device generating a data frame detection signal if the input data written into the shift register is identical to the stored data frame synchronization data pattern.

18. The high speed processor as claimed in claim 17, wherein after the data frame detection signal generated, the shift register is expanded to form a toroidal memory for buffering the xDSL data.

19. The high speed processor as claimed in one of the preceding claims, wherein the output interface buffer (26) is a PCM interface buffer for buffering PCM data.

20. The high speed processor as claimed in one of the preceding claims, wherein each internal register (14) has a plurality of memory locations for different data words.

21. The high speed processor as claimed in one of the preceding claims, wherein each processor task executed by the data processing unit (13) is assigned a separate internal register.

22. The high speed processor as claimed in one of the preceding claims, wherein peripherals can be connected to the interface buffers (9, 26).

23. The high speed processor as claimed in one of the preceding claims, wherein the input interface buffer (9) and the output interface buffer (26) can be configured.